

Fig. 1 ¹⁰ Instruction Execution Unit (IEU)

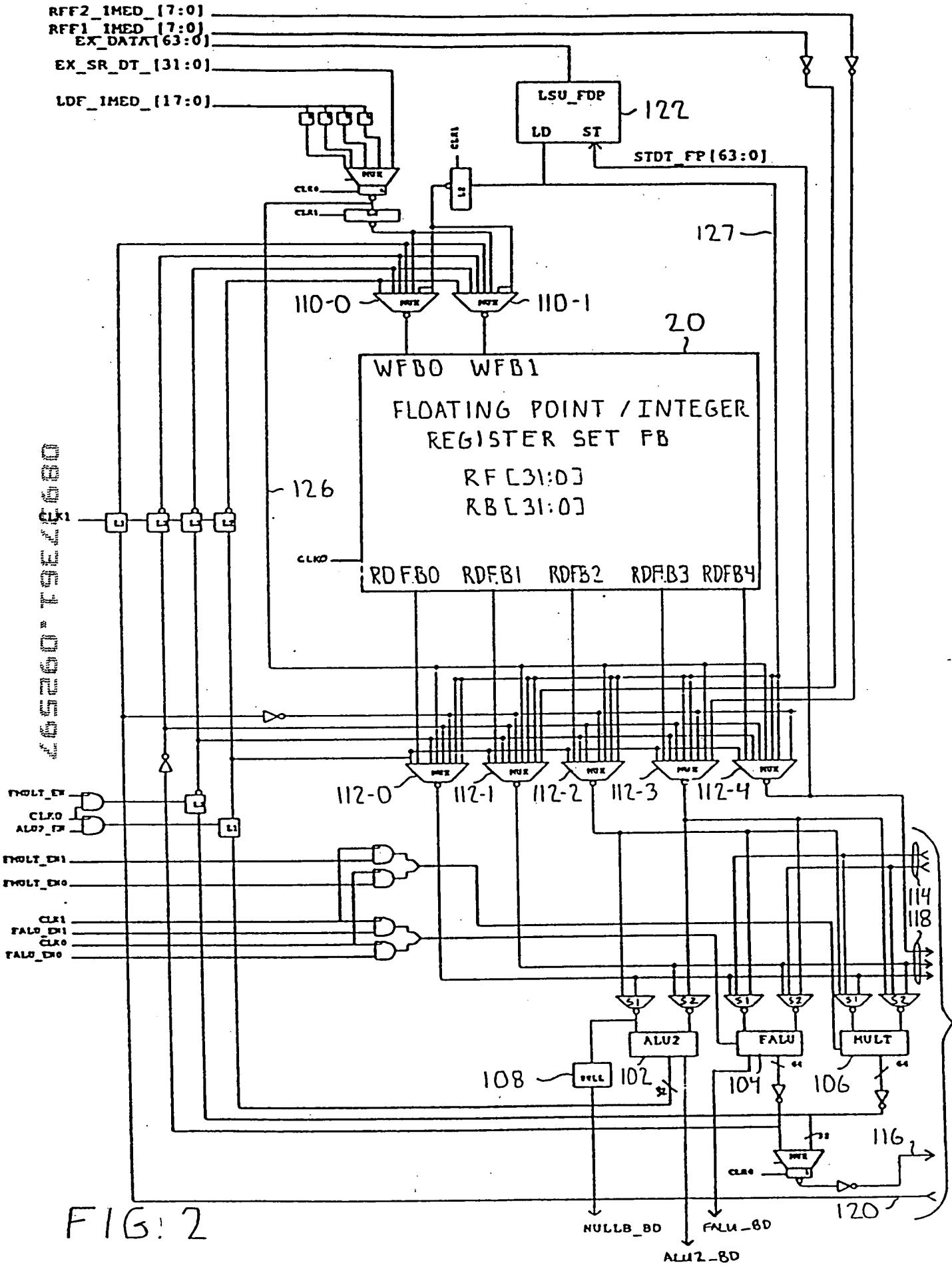


FIG: 2

Control Bit (PSR[7])

CLK0

T0 / FROM FIG. 2

EX_SR_DT[31:0]

EX_TADR[31:0]

NULLA_BD

EX_VM_ADR[31:0]

RFA2_IMED[16:0]
RFA1_IMED[15:0]

LDI_IMED[15:0]

IF_PC[31:0]
CF_OFFSET[5:0]

EX_DATA[63:0]

LSU_IDP

LO ST

152

EX_SR_DT[31:0]

CLR0

CLR1

32

MUX

148-0 148-1

18

154

WA0 WA1

INTEGER REG. SET A
RA[31:0]

RDAO RDA1 RDA2 RDA3 RDA4

12 32

150-0 150-1 150-2 150-3 150-4

114

118

116

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140 ALU0

142 ALU1

144 SHFO

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140 ALU0_BD

142 ALU1_BD

144 SHFO_BD

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140 ALU0_EX

142 ALU1_EX

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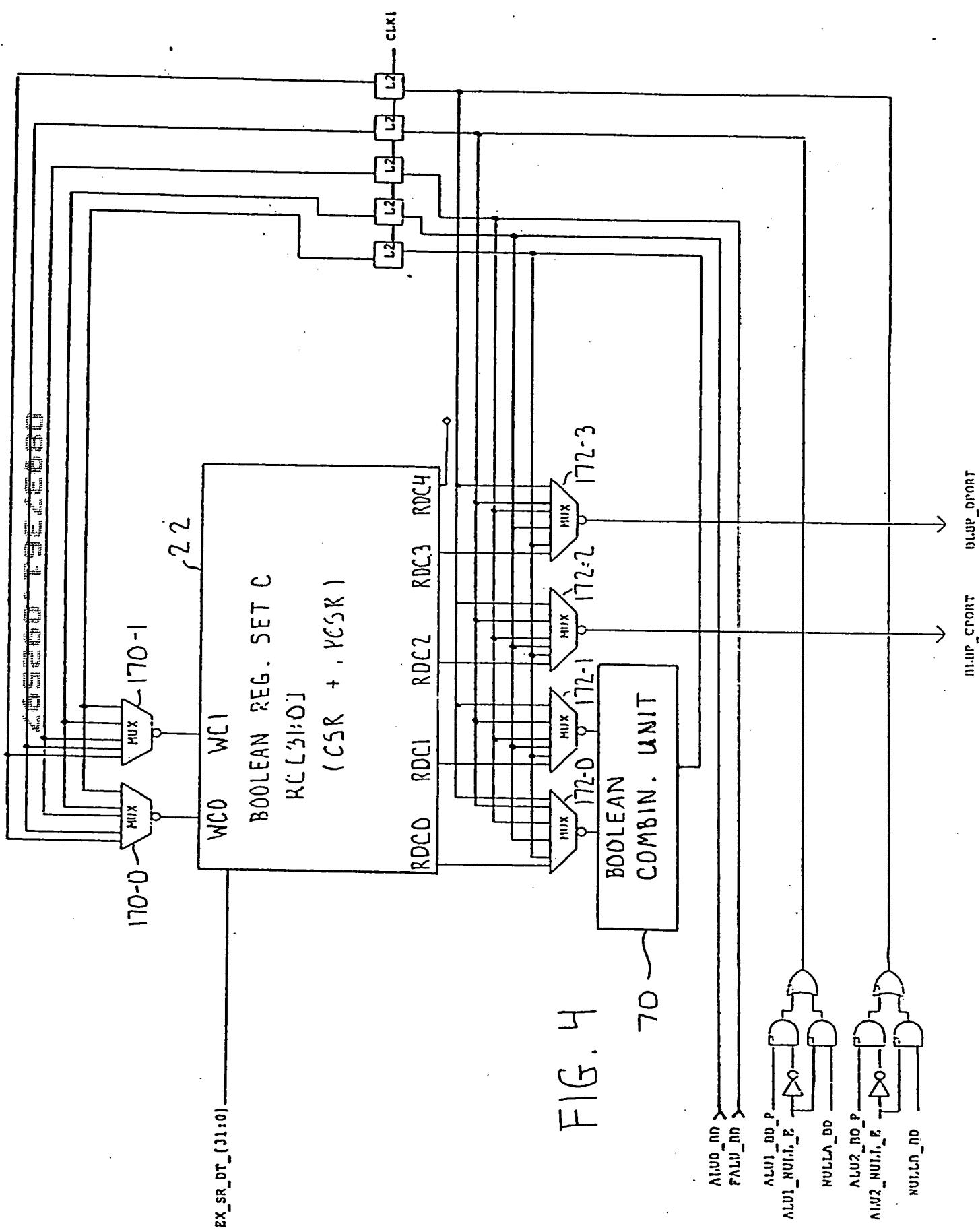
118

140 ALU0_EX

142 ALU1_EX

144 SHFO_EX

146



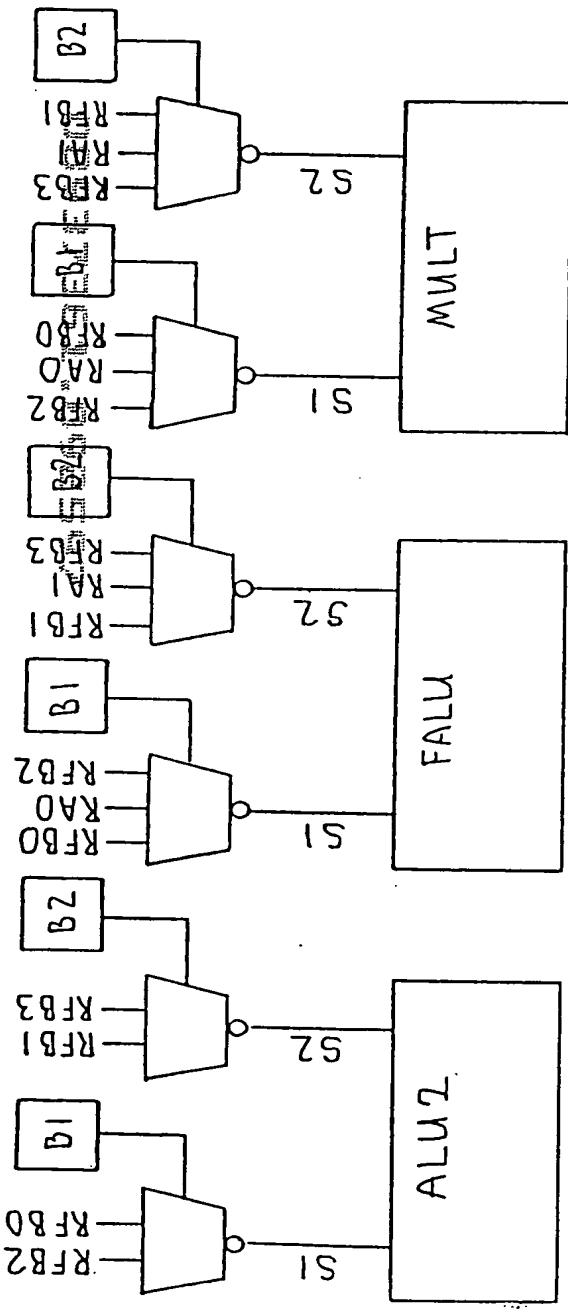


FIG.

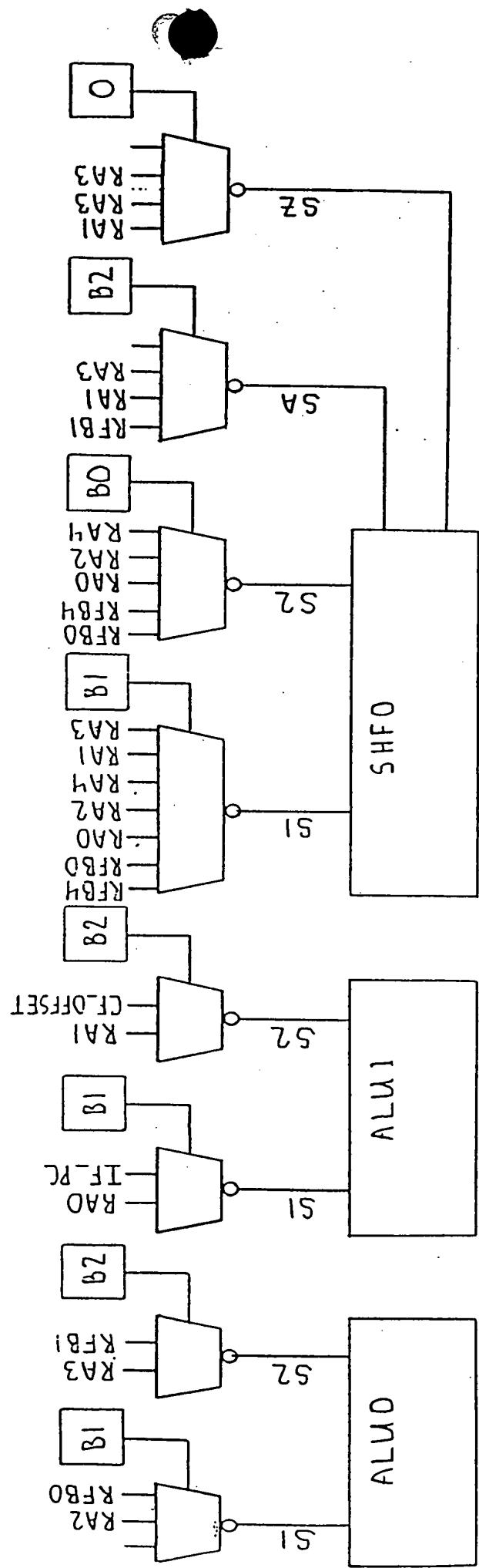


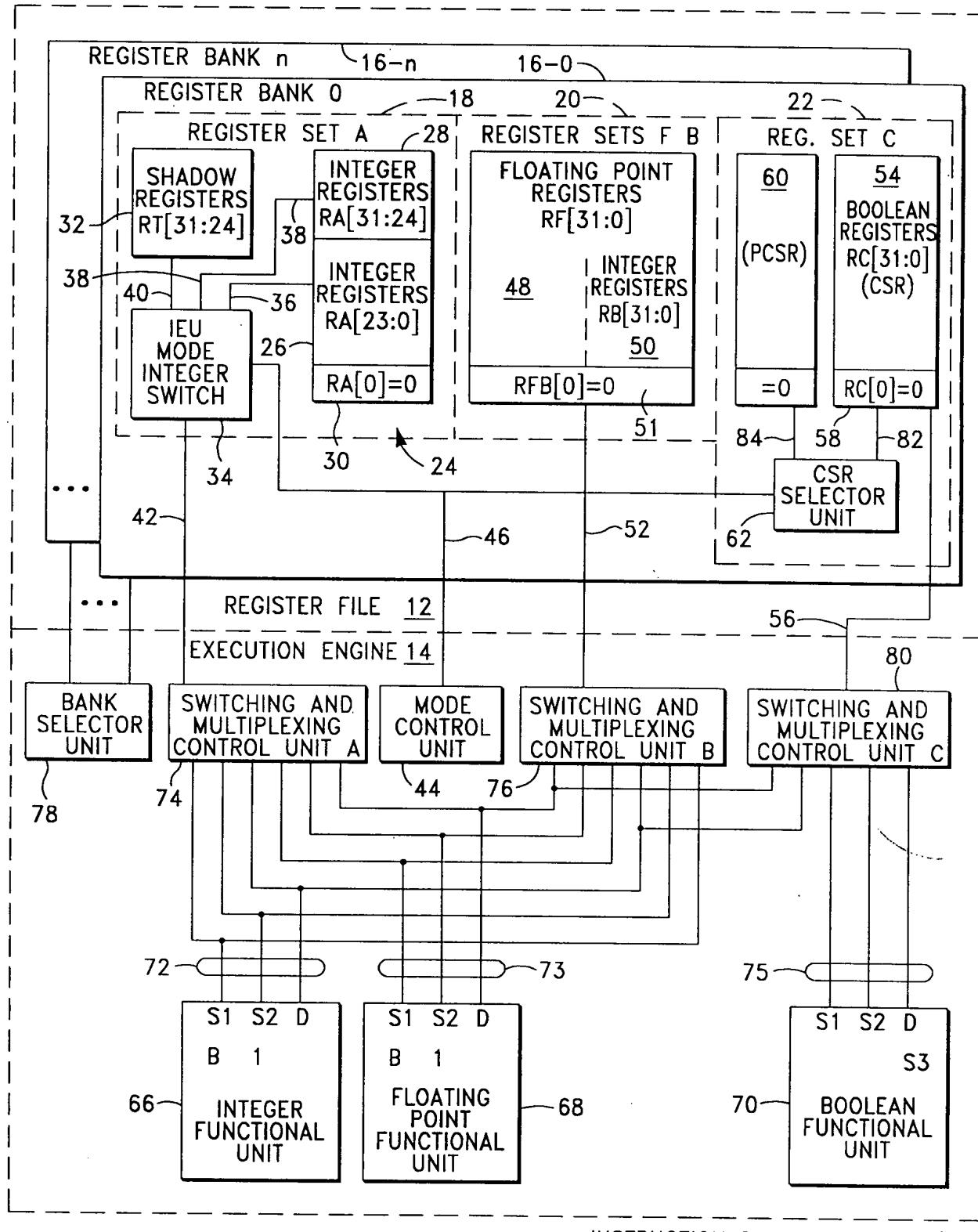
FIG. 6

INSTRUCTION FORMAT

RESERVED	31
INSTRUCTION CLASS	30 29 28 27 26 25 24 23 22 21 20
B0 (DEST.)	25 24 23 22 21 20
OPCODE	24 23 22 21 20
ADDRESSING MODE	21 20
DESTINATION REGISTER	16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
B1 (SOURCE 1)	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
SOURCE REGISTER 1	14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
FUNCTION SELECT	13 12 11 10 9 8 7 6 5 4 3 2 1 0
RESERVED	12 11 10 9 8 7 6 5 4 3 2 1 0
B2 (SOURCE 2)	11 10 9 8 7 6 5 4 3 2 1 0
SOURCE REGISTER 2	10 9 8 7 6 5 4 3 2 1 0

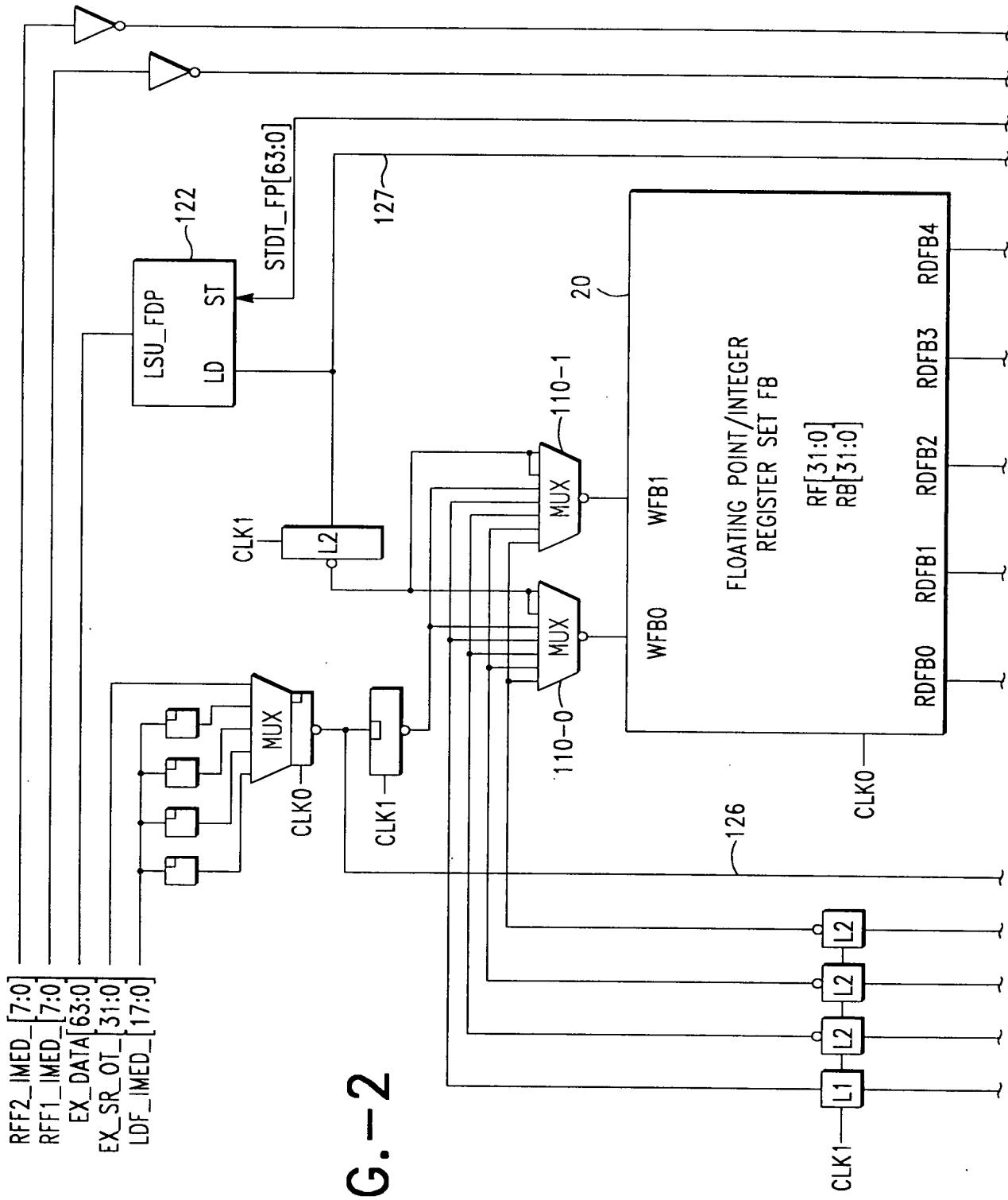
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FIG.-1



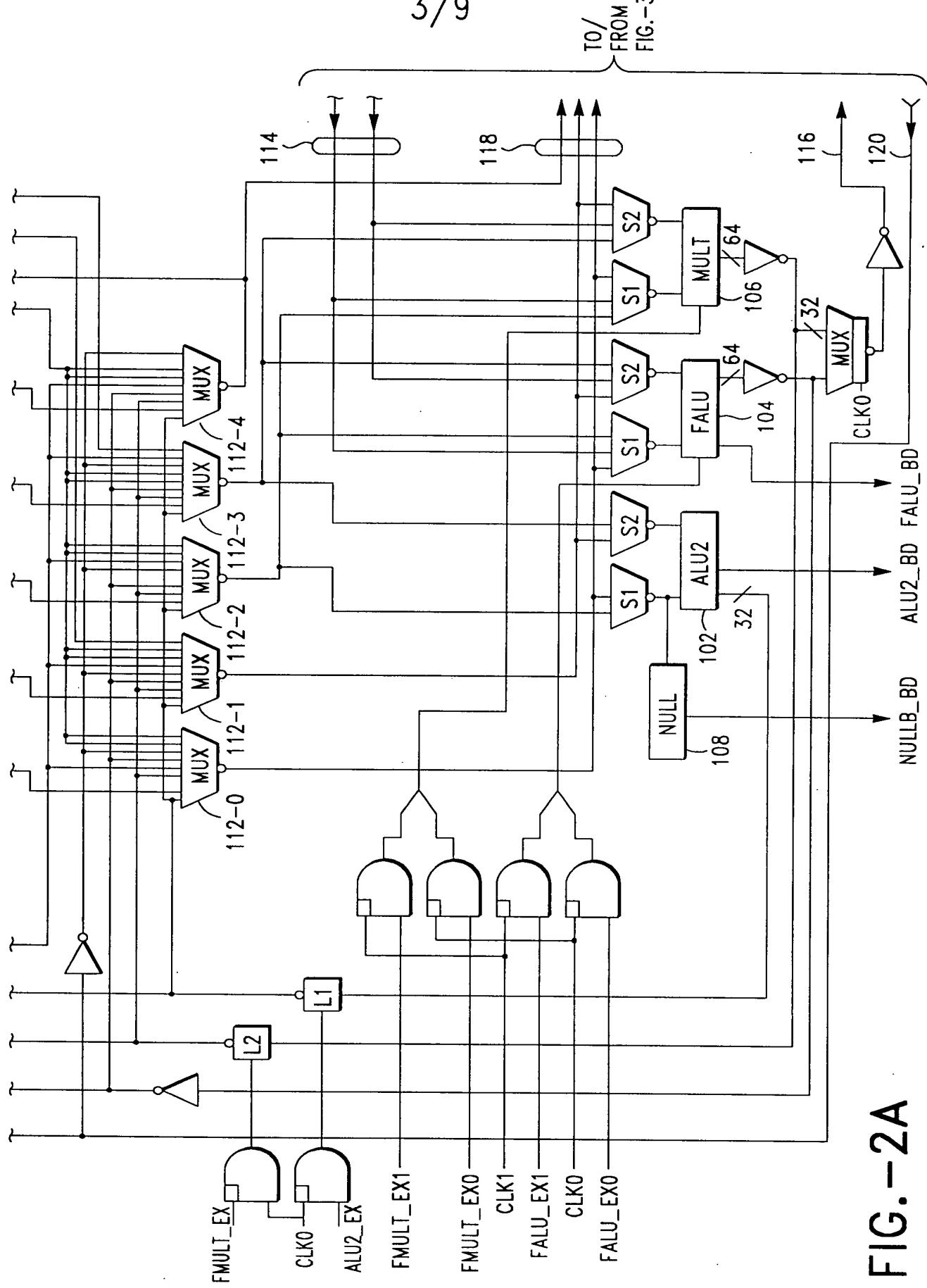


FIG.-2A

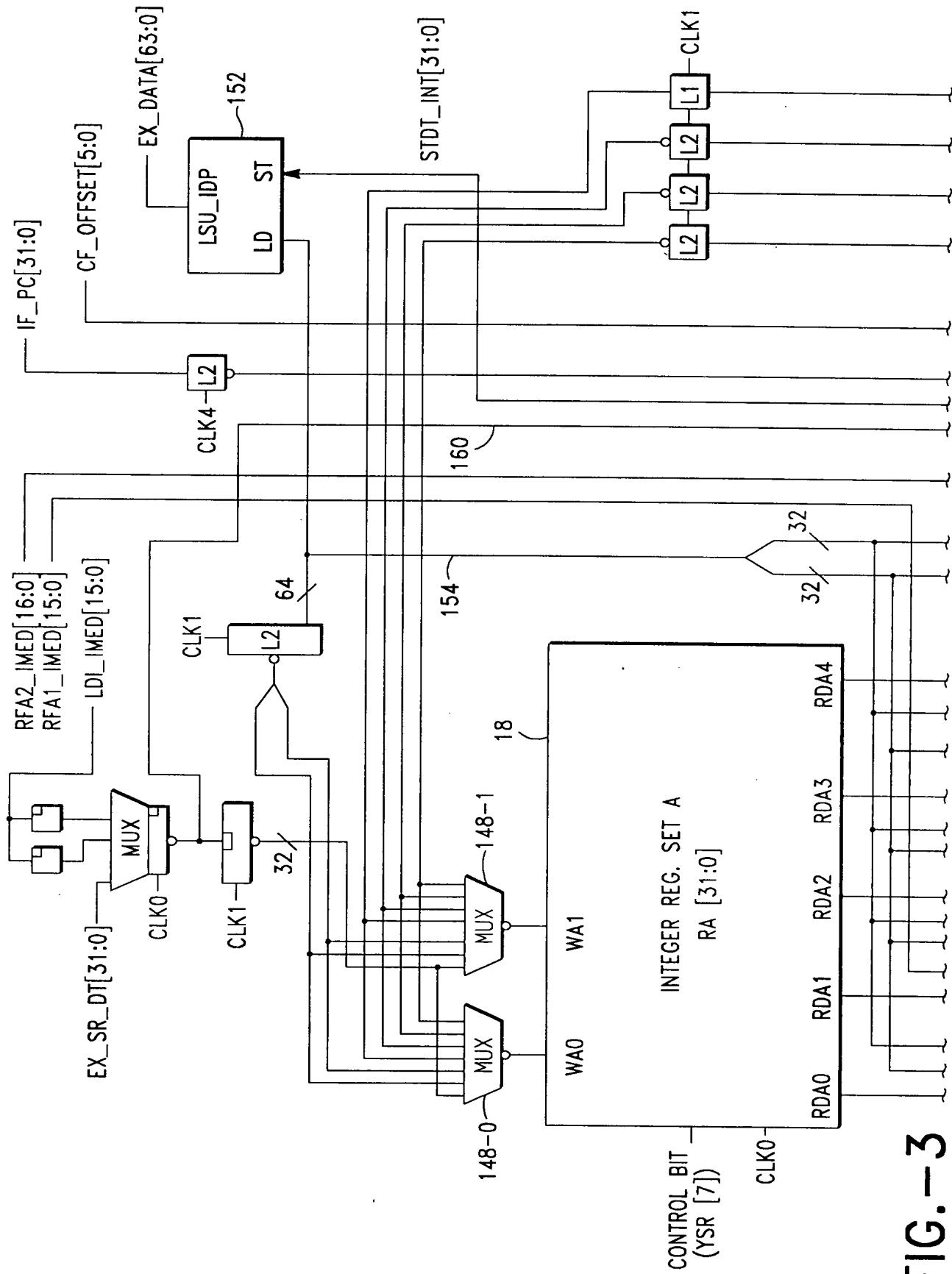
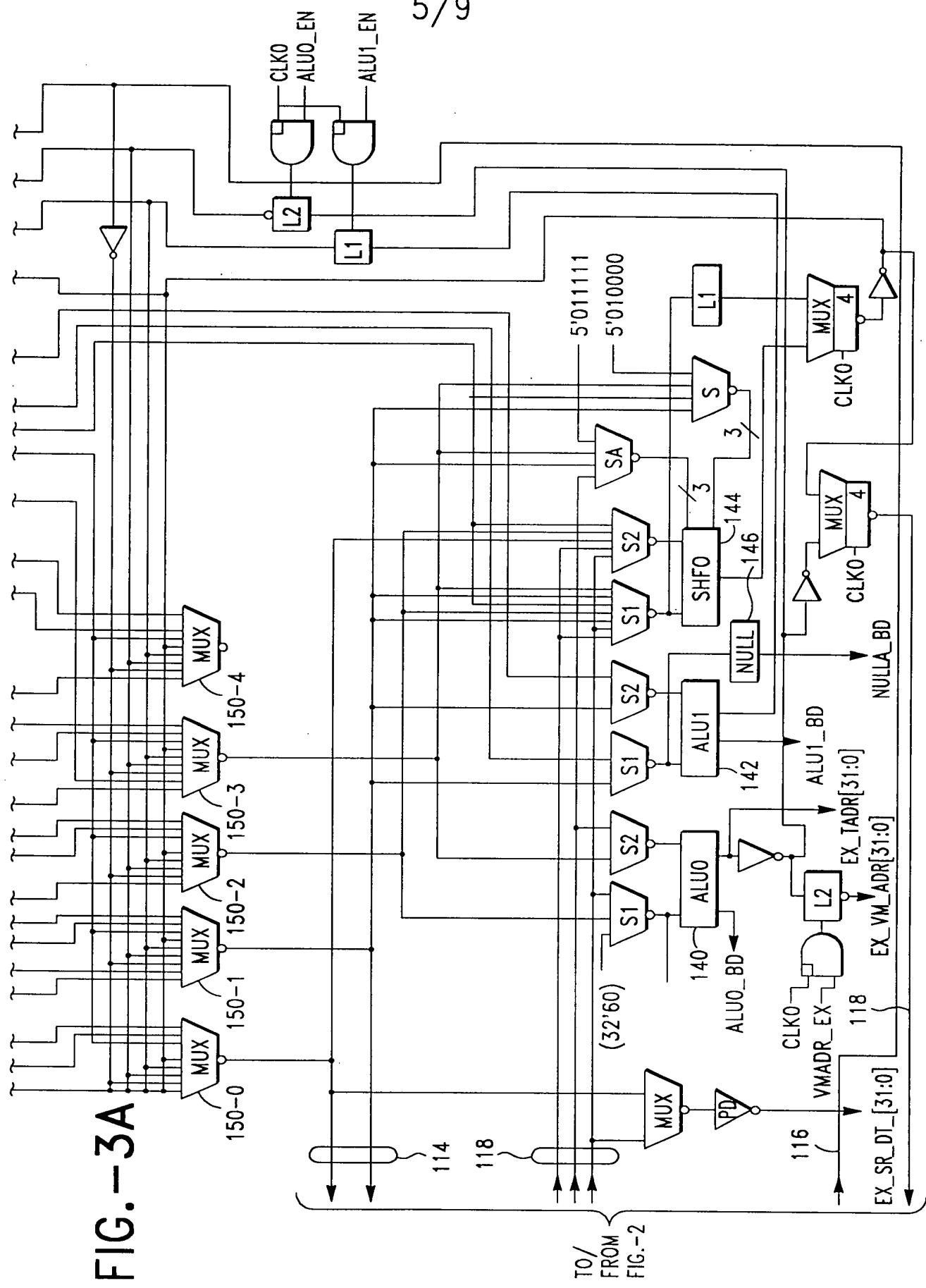


FIG.-3



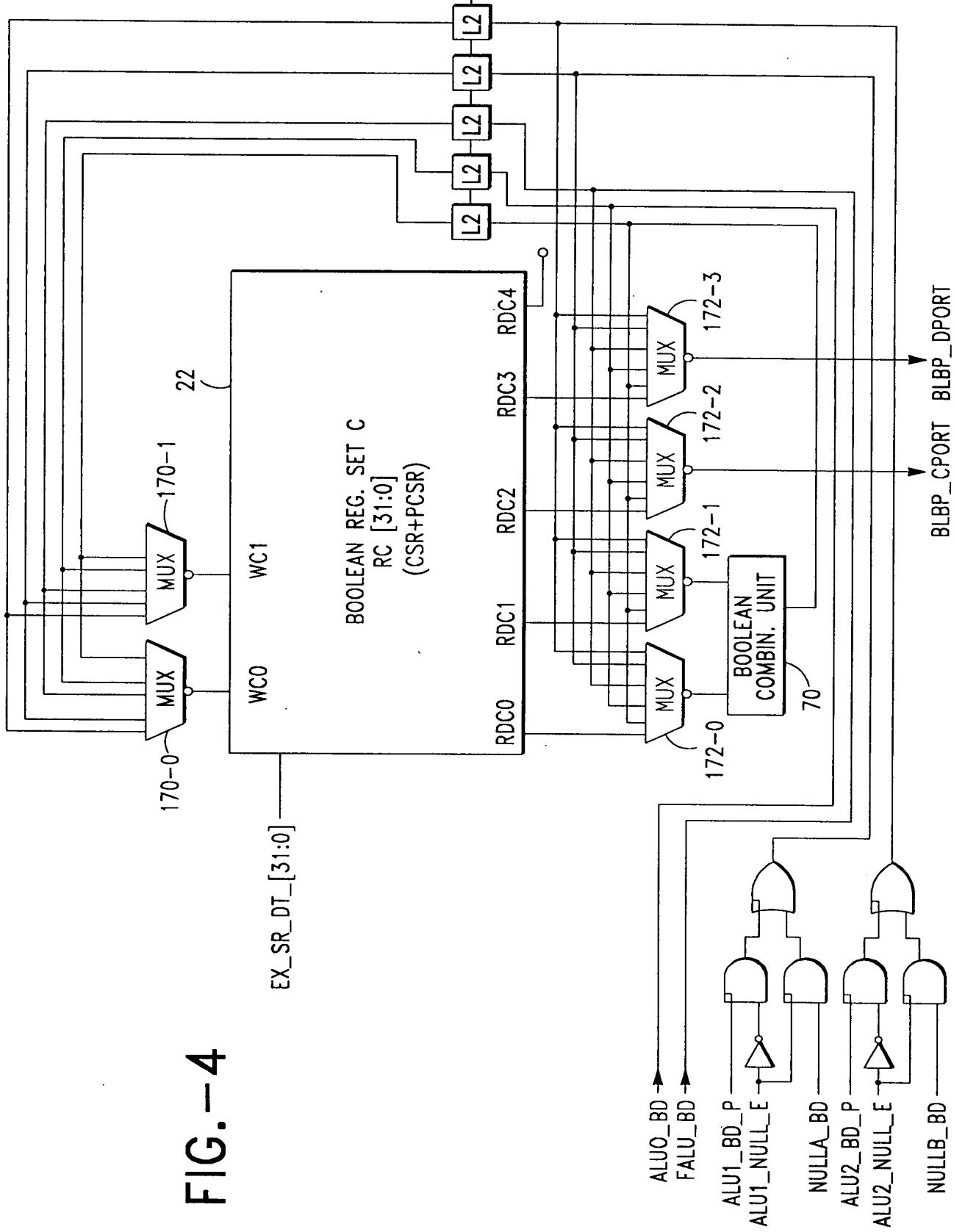


FIG. - 4

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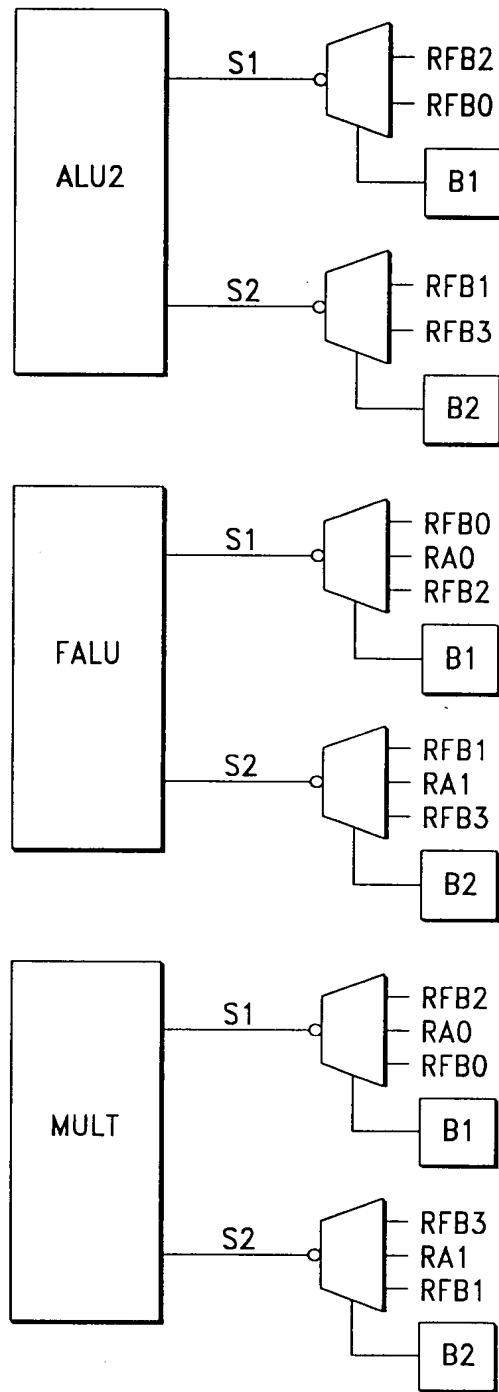


FIG.-5

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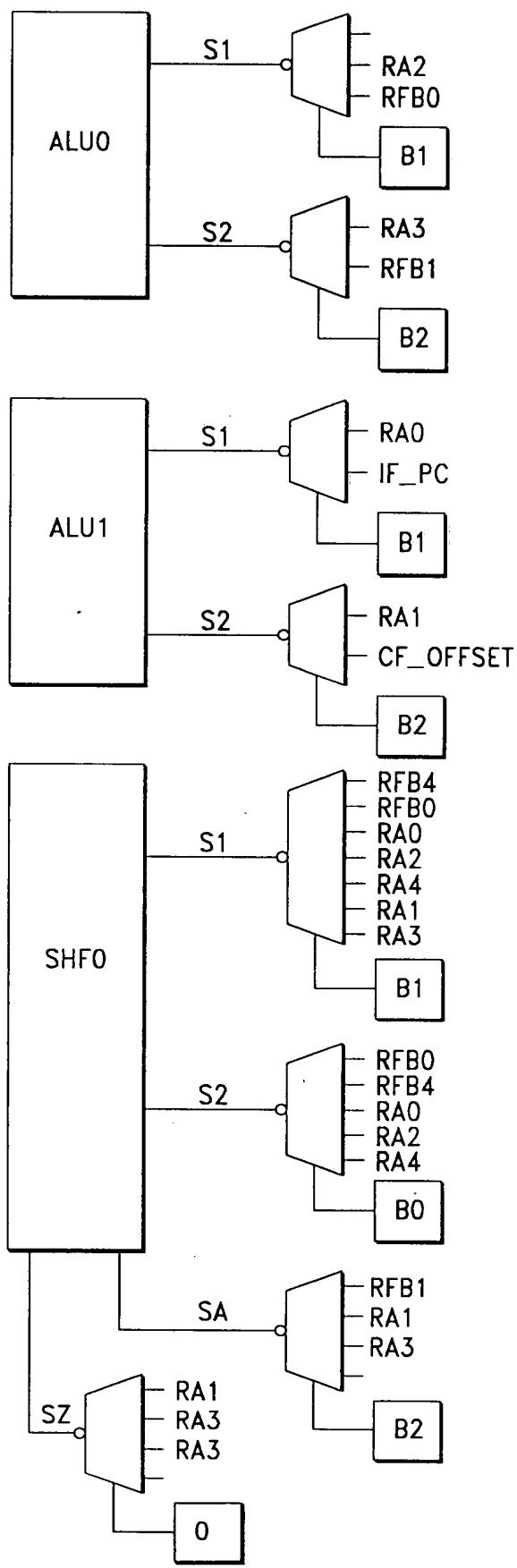


FIG.-6

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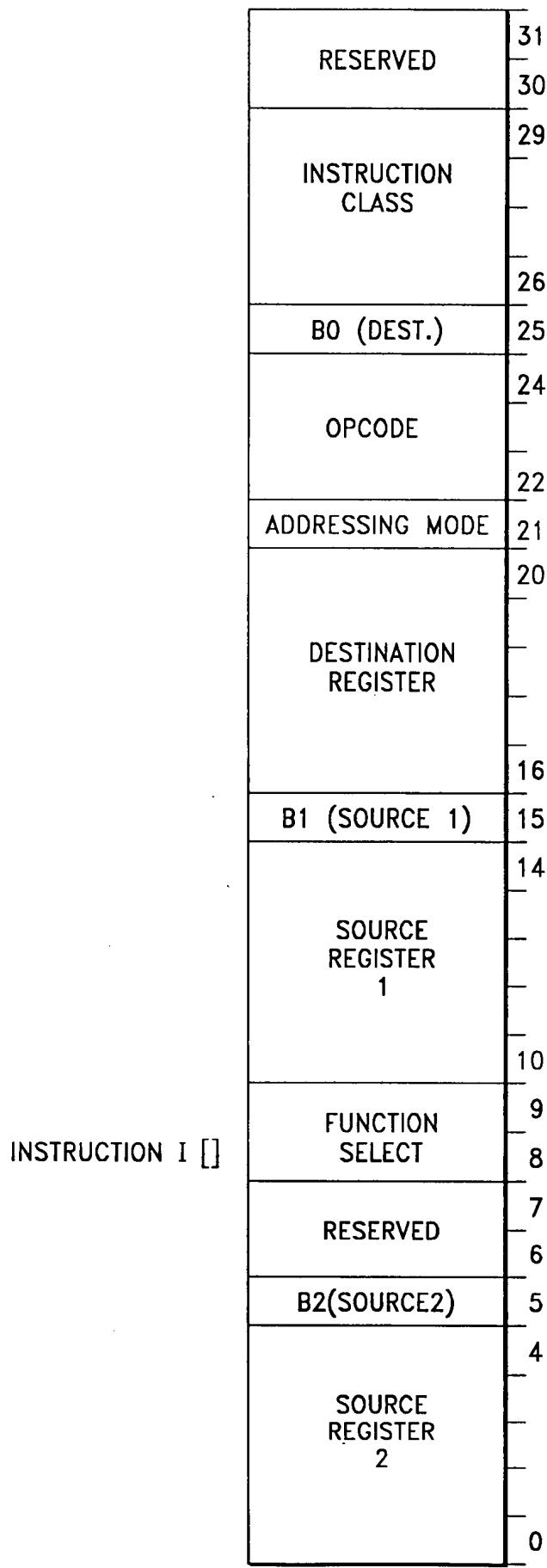


FIG.-7